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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,623	08/01/2003	Kouji Takahashi	14225-019001 / F1030316US	4757

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/632,623	TAKAHASHI ET AL.
	Examiner	Art Unit
	Victor A. Mandala Jr.	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *18-21* is/are withdrawn from consideration.

5)☒ Claim(s) *15-17* is/are allowed.

6)☒ Claim(s) *1,3 and 7-14* is/are rejected.

7)☒ Claim(s) *2 & 4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Japanese Reference*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, & 7-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent No. 2001-352034 Sakamoto et al. (Japanese Patent Office Computer Translation).

1. Referring to claim 1, a circuit device comprising: a semiconductor element, (Figure 9A #52A), is mounted a die pad, (Figure 9A #51A), on which with a brazing material, (Figure 9A & Paragraph 0065 and 0067-0069), a bonding pad, (Figure 9A #51B), disposed in close vicinity to the die pad, (Figure 9A #51A), plating films, (Figure 9A & Paragraph 0065 and 0067-0069), formed on a surface of the a surface of the bonding pad, (Figure 9A #51B), respectively, die pad, (Figure 9A #51A), and on wherein a second plating film, (Figure 9A on the right side of #52A bonding pad #51B), is disposed apart from a first plating film, (Figure 9A on #51A and the left side of #52A bonding pad #51B & Paragraph 0065 and 0067-0069), on which the semiconductor element, (Figure 9A #52A), of the die pad, (Figure 9A #51A), is mounted.

2. Referring to claim 3, a circuit device, wherein the second plating film, (Figure 9A on the right side of #52A bonding pad #51B & Paragraph 0065 and 0067-0069), prevents the brazing material, (Figure 9A & Paragraph 0065 and 0067-0069), that has overflowed from the first plating film, (Figure 9A on #51A and the left side of #52A bonding pad

#51B & Paragraph 0065 and 0067-0069), from flowing out by a space, (Figure 9A between #51A and the right #51B bonding pad), between the first, (Figure 9A on #51A and the left side of #52A bonding pad #51B & Paragraph 0065 and 0067-0069), and second plating films, (Figure 9A on the right side of #52A bonding pad #51B & Paragraph 0065 and 0067-0069).

3. Referring to claim 7, a circuit device, wherein the semiconductor device is an IC chip, (Paragraph 0064).

4. Referring to claim 8, a circuit device, wherein the semiconductor element is electrically connected to a desired bonding pad, (Figure 9A #51B), among the bonding pads through a fine metal wire, (Figure 9A #55A).

5. Referring to claim 9, a circuit device comprising: a die pad on which a semiconductor element, (Figure 9A #52A), is mounted, a first bonding pad, (Figure 9A #51B), disposed in close vicinity to the die pad, (Figure 9A #51A), and electrically separated from the die pad, (Figure 9A #51A), a second bonding pad, (Figure 9A #51B), disposed in close vicinity to the die pad, (Figure 9A #51A), and formed integrally, (Figure 9A #53A), with the die pad, (Figure 9A #51A), and an insulating resin, (Figure 7A #50), for sealing the semiconductor element, (Figure 9A #52A), the die pad, (Figure 9A #51A), the first bonding pad, (Figure 9A #51B), and the second bonding pad, (Figure 9A #51B), while exposing a back surface of the die pad, (Figure 9A #51A), a back surface of the first bonding pad, (Figure 9A #51B), and a back surface of the second bonding pad, (Figure 9A #51B), wherein the second bonding pad, (Figure 9A #51B), is connected to the die pad, (Figure 9A #51A), through a wiring portion narrow in width, (Figure 9A #55A).

6. Referring to claim 10, a circuit device, wherein an area in which the second bonding pad, (Figure 9A #51B), is in contact with the insulating resin, (Figure 9A #50), is increased by providing the wiring portion, (Figure 9A #55A), so that joining is strengthened between the bonding pad, (Figure 9A #51B), and the insulating resin, (Figure 9A #50).

7. Referring to claim 11, a circuit device, wherein a plurality of the first bonding pads, (Figure 9A #51B), are disposed along opposite sides the die pad, (Figure 9A #51A).

8. Referring to claim 12, a circuit device, wherein a plurality of the second bonding pads, (Figure 9A #51B), are disposed along the opposite sides of the die pad, (Figure 9A #51A).

9. Referring to claim 13, a circuit device, wherein the semiconductor element, (Figure 9A #52A), is electrically connected to a desired first bonding pad, (Figure 9A #51B), among the first bonding pads, (Figure 9A #51B), and to a desired second bonding pad, (Figure 9A #51B), among the second bonding pads, (Figure 9A #51B), through fine metal wires, (Figure 9A #55A).

10. Referring to claim 14, a circuit device of Claim 9, wherein the first bonding pad, (Figure 9A #51B), and the second bonding pad, (Figure 9A #51B), are formed circularly, (having a radius around the center of the device, thus formed circularly around #52A).

Allowable Subject Matter

11. Claims 2, 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Claims 15-17 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
05/05/05